Exhibit 35

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Paper 11
Entered: March 11, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

EMC CORPORATION,
Petitioner,

v.

ACQIS LLC,
Patent Owner.

Case IPR2014-01469
Patent RE42,814 E

Before MICHAEL P. TIERNEY, MICHAEL J. FITZPATRICK, and ROBERT J. WEINSCHENK, *Administrative Patent Judges*.

WEINSCHENK, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

EMC Corporation ("Petitioner") filed a Petition (Paper 2; "Pet." or "Petition") requesting *inter partes* review of claims 24 and 31–33 of U.S. Patent No. RE42,814 E (Ex. 1001; "the '814 patent"). ACQIS LLC ("Patent Owner") filed a Preliminary Response to the Petition. Paper 7 ("Prelim. Resp."). We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

For the reasons set forth below, on this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing the unpatentability of claims 24 and 31–33 of the '814 patent. Accordingly, we institute *inter partes* review as to claims 24 and 31–33 of the '814 patent on the grounds specified below.

A. *Related Proceedings*

The parties indicate that the '814 patent is at issue in the following district court cases: *ACQIS LLC v. Alcatel-Lucent USA, Inc.*, No. 6:13-cv-00638 (E.D. Tex.); *ACQIS LLC v. EMC Corp.*, No. 6:13-cv-00639 (E.D. Tex.); *ACQIS LLC v. Ericsson, Inc.*, No. 6:13-cv-00640 (E.D. Tex.); and *ACQIS LLC v. Huawei Technologies Co.*, No. 6:13-cv-00641 (E.D. Tex.). Pet. 56; Paper 5, 2.

Petitioner identifies the following *inter partes* review proceedings as being related to this proceeding (Pet. 57):

IPR Case No.	Involved U.S. Patent No.
IPR2014-01452	RE43,171 E
IPR2014-01462	8,041,873 B2

B. *The '814 Patent*

The '814 patent is a reissue of U.S. Patent No. 6,321,335 ("the '335 patent"). *See* Ex. 1001. The '335 patent relates to securing a personal computer with password protection techniques. *Id.* at col. 1, ll. 41–44. The reissue application that issued as the '814 patent added Figures 8–18, the written description at column 11, line 49 to column 25, line 51, and claims 24–53. *Id.* at col. 4, ll. 35–58, col. 11, l. 49–col. 32, l. 50. The figures, written description, and claims added during reissue relate to interfacing two Peripheral Component Interconnect ("PCI") buses using a non-PCI channel. *Id.* at col. 19, ll. 31–33, Fig. 11. More specifically, PCI address and data bits are encoded and then converted from a parallel format to a serial format. *Id.* at col. 20, ll. 62–65, Figs. 12A, 12B. The information is transmitted in a serial format over a non-PCI channel, and, when received, the information is converted back into a parallel format and decoded so it is suitable for transmission on a PCI bus. *Id.* at col. 20, ll. 65–67, Figs. 13A, 13B.

C. *Illustrative Claim*

Claims 24 and 31 are independent. Claim 24 is illustrative and is reproduced below.

> 24. A method for operating a computer system, said method comprising:
>
> inserting an attached computer module ("ACM") into a bay of a console in a modular computer system, the console comprising a first low voltage differential signal (LVDS) channel comprising two unidirectional serial channels that transmit encoded data of Peripheral Component Interconnect (PCl) bus transaction in opposite directions; said ACM comprising
>
> a microprocessor unit coupled to a mass memory storage device;

> a north bridge to communicate address and data bits of PCI bus transaction in serial form, said north bridge directly coupled to said microprocessor unit;
>
> a main memory coupled to said microprocessor unit through said north bridge; and
>
> a second LVDS channel comprising two unidirectional serial channels that transmit data in opposite directions, said second LVDS channel extending from said north bridge to convey said address and data bits of PCI bus transaction in serial form;
>
> applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device; and
>
> prompting for a user password from a user on a LCD display coupled to the console.

Id. at col. 26, ll. 18–43.

D. *References*

Petitioner relies on the following references and declaration (*see* Pet. 58–59):

Reference or Declaration	Exhibit No.
U.S. Patent No. 5,608,608 ("Flint")	Ex. 1002
Declaration of Bruce Young	Ex. 1003
Robert W. Horst, TNet: A Reliable System Area Network ("Horst")	Ex. 1009
U.S. Patent No. 6,148,357 ("Gulick")	Ex. 1010
A. Bogaerts et al., RD24 Status Report: Application of the Scalable Coherent Interface to Data Acquisition at LHC ("Bogaerts")	Ex. 1011
U.S. Patent No. 6,012,145 ("Mathers")	Ex. 1014
U.S. Patent No. 5,961,623 ("James")	Ex. 1018
National Semiconductor, LVDS Owner's Manual: Design Guide ("LVDS Owner's Manual")	Ex. 1019

E. *Asserted Grounds of Unpatentability*

Petitioner asserts that the challenged claims are unpatentable on the following grounds[1] (*see* Pet. 58–59):

Claims Challenged	Basis	References
24 and 31–33	35 U.S.C. § 103(a)	Flint, Gulick, and Mathers
24 and 31–33	35 U.S.C. § 103(a)	Horst and Mathers
24 and 31–33	35 U.S.C. § 103(a)	Bogaerts, Gulick, Mathers, and James
24 and 31–33	35 U.S.C. § 103(a)	Any of the grounds above and LVDS Owner's Manual

II. ANALYSIS

A. *Claim Construction*

The claims of an unexpired patent are interpreted using the broadest reasonable interpretation in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). On this record and for purposes of this decision, the only claim terms requiring express construction are the terms "Peripheral Component Interconnect (PCI) bus transaction" and "PCI bus transaction."

Petitioner proposes construing the term "Peripheral Component Interconnect (PCI) bus transaction" in the challenged claims to mean "a data signal communication with an interconnected peripheral component." Pet. 13. Petitioner argues that its proposed construction is supported by a

[1] Patent Owner argues that the obviousness combinations are asserted in the alternative, and, thus, should be denied. Prelim. Resp. 25–33. The decisions cited by Patent Owner in support of that argument are not binding precedent and do not require that alternative combinations be denied, and we do not deny any grounds asserted in the Petition on that basis.

decision of the U.S. District Court for the Eastern District of Texas construing a similar term in related, but different, patents. *Id.* at 12–13. Patent Owner proposes construing the term "Peripheral Component Interconnect (PCI) bus transaction" in the challenged claims to mean "command, address, and data information, in accordance with the PCI standard, for communication with an interconnected peripheral component." Prelim. Resp. 5. Patent Owner argues that its proposed construction is supported by the claim language, the specification of the '814 patent, and certain extrinsic evidence. *Id.* at 5–13. The dispute between the parties focuses on whether the term "Peripheral Component Interconnect (PCI)" refers to the PCI industry standard.

On this record and for purposes of this decision, we agree with Patent Owner that the term "Peripheral Component Interconnect (PCI)" refers to the PCI industry standard. Industry literature and dictionaries use the proper noun "Peripheral Component Interconnect" and the abbreviation "PCI" to refer to a particular industry specification for a local bus. *See, e.g.*, Ex. 2001, 1; Ex. 2002, 6–7; Ex. 2003, 7–8. The challenged claims also recite "Peripheral Component Interconnect" as a proper noun and abbreviate it as "PCI" (Ex. 1001, col. 27, ll. 24–25, col. 28, ll. 35–36), indicating that the challenged claims use those terms consistent with the understood industry meaning. *See Azure Networks, LLC v. CSR PLC*, 771 F.3d 1336, 1348 (Fed. Cir. 2014). The specification of the '814 patent also supports Patent Owner's proposed construction. For example, the specification uses the common noun "peripheral bus" when referring generally to a peripheral bus. *See, e.g.*, Ex. 1001, col. 7, ll. 4–6 ("Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and *a peripheral*

bus.") (emphasis added). Thus, the challenged claims could have used the term "peripheral component bus transaction," but instead recite a "Peripheral Component Interconnect (PCI) bus transaction." Further, Petitioner's declarant in this proceeding, Mr. Bruce Young, admits that the term "Peripheral Component Interconnect (PCI)" refers to an industry standard (Ex. 1003 ¶ 58), and Petitioner admits the same in the related district court case (Ex. 2006, 1, 3).

The only evidence Petitioner offers in support of its proposed construction is the claim construction order issued in *ACQIS LLC v. Appro International, Inc.*, No. 6:09-cv-00148 (E.D. Tex. Feb. 3, 2011). Pet. 12–13; Ex. 1013. In that case, the district court considered related, but different, patents. Pet. 12. Also, the parties in that case did not appear to dispute that the term "Peripheral Component Interconnect (PCI)" refers to an industry standard. Rather, the dispute before the district court focused on which particular bus architectures of the PCI industry standard were covered by the term "PCI bus transaction." Ex. 1013, 7 ("The parties' primary dispute is whether the term is limited to the conventional, parallel PCI Local Bus, and, therefore excludes PCI Express bus architecture and bus transaction protocol.").

Therefore, on this record and for purposes of this decision, the broadest reasonable interpretation of the claim terms "Peripheral Component Interconnect (PCI) bus transaction" and "PCI bus transaction" is "Peripheral Component Interconnect (PCI) industry standard bus transaction."

B. *Asserted Grounds of Unpatentability*

1. *Obviousness of Claims 24 and 31–33 over Flint, Gulick, and Mathers*

Petitioner argues that claims 24 and 31–33 would have been obvious over Flint, Gulick, and Mathers. Pet. 59. Flint relates to a cartridge-based design for computers. Ex. 1002, col. 2, ll. 18–21. We have reviewed Petitioner's assertions and supporting evidence, and, for the reasons discussed below, Petitioner does *not* demonstrate a reasonable likelihood of prevailing in showing that claims 24 and 31–33 would have been obvious over Flint, Gulick, and Mathers.

Each independent claim challenged by Petitioner recites a bridge to communicate address and data bits of a PCI bus transaction. Ex. 1001, col. 27, ll. 29–30, col. 28, ll. 34–39. Petitioner argues that Flint teaches this limitation because the local bus interface 218 communicates "with a number of peripheral components in the chassis and cartridge through the I/O interface, an expansion bus interface, and PCMCIA interfaces via the common bus (220, 300, 102)." Pet. 20. Petitioner does not argue that Flint teaches communicating address and data bits of a PCI industry standard bus transaction, or that doing so would have been obvious based on Flint. *Id.* at 20–23. Petitioner's argument instead is premised on the claim term "PCI bus transaction" being construed to refer to a communication with any interconnected peripheral component. *Id.*; Prelim. Resp. 10. For the reasons discussed above, the claim term "PCI bus transaction" refers to the PCI industry standard. *See* Section II.A. Therefore, on this record, Petitioner does *not* demonstrate a reasonable likelihood of prevailing in showing that claims 24 and 31–33 would have been obvious over Flint, Gulick, and

Mathers.[2]

2. *Obviousness of Claims 24 and 31–33 over Horst and Mathers*

Petitioner argues that claims 24 and 31–33 would have been obvious over Horst and Mathers. Pet. 59. Horst relates to a system area network called TNet that is designed for reliable, efficient communications among processors and peripherals. Ex. 1009, 1. We have reviewed Petitioner's assertions and supporting evidence, and, for the reasons discussed below, Petitioner does *not* demonstrate a reasonable likelihood of prevailing in showing that claims 24 and 31–33 would have been obvious over Horst and Mathers.

Each independent claim challenged by Petitioner recites a low voltage differential signal (LVDS) channel. Ex. 1001, col. 27, ll. 22–23, col. 28, l. 25. Petitioner argues that "Horst teaches that TNet links include low voltage, differential ECL data links (*i.e.*, a LVDS channel)" and cites generally to pages 3 and 4 of Horst as support for that argument. Pet. 33. Horst discloses that "[i]ntercabinet links use differential emitter-coupled logic drivers to drive up to 20 meters of cable." Ex. 1009, 4. However, Petitioner does not identify with specificity anything in Horst that teaches that the differential emitter-coupled logic drivers are *low voltage*, and Petitioner does not argue that it would have been obvious from Horst that the differential emitter-coupled logic drivers were *low voltage*. Pet. 33; Ex. 1003 ¶¶ 76, 145, 159[24B]. Petitioner instead admits that later implementations of the TNet system (not the one disclosed in Horst) use

[2] Petitioner does not argue that it would have been obvious to combine a PCI bus transaction feature from Gulick or Mathers with Flint. Pet. 20–23.

LVDS signaling. Pet. 33. Therefore, on this record, Petitioner does *not* demonstrate a reasonable likelihood of prevailing in showing that claims 24 and 31–33 would have been obvious over Horst and Mathers.

3. *Obviousness of Claims 24 and 31–33 over Horst, Mathers, and LVDS Owner's Manual*

Petitioner argues that claims 24 and 31–33 would have been obvious over Horst, Mathers, and the LVDS Owner's Manual. Pet. 59. We have reviewed Petitioner's assertions and supporting evidence, and, for the reasons discussed below, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claims 24 and 31–33 would have been obvious over Horst, Mathers, and the LVDS Owner's Manual.

a. *Claim 24*

Independent claim 24 recites "inserting an attached computer module ("ACM") into a bay of a console in a modular computer system." Ex. 1001, col. 27, ll. 20–21. Petitioner identifies the processor node in Horst as being the ACM, and the cabinet in Horst as being the console. Pet. 30. Petitioner argues that the processor node in Horst connects with the cabinet through a backplane. *Id.*; Ex. 1009, 1. On this record, Petitioner has shown sufficiently that Horst teaches the above limitation of claim 24.

Independent claim 24 recites "the console comprising a first low voltage differential signal (LVDS) channel comprising two unidirectional serial channels that transmit . . . in opposite directions." Ex. 1001, col. 27, ll. 21–26. Petitioner argues that the cabinet in Horst comprises byte-serial data links with independent transmit and receive channels to transmit data in opposite directions. Pet. 32–33; Ex. 1009, 3, Figs. 3, 4, 8. Petitioner also argues that the byte-serial data links in Horst comprise differential emitter-coupled logic drivers. Pet. 33; Ex. 1009, 4, Fig. 4. However, as discussed

above in Section II.B.2, Petitioner does not identify with specificity anything in Horst that teaches that the byte-serial data links are *low voltage*. Pet. 33; Ex. 1003 ¶¶ 76, 145, 159[24B]. Petitioner argues that the LVDS Owner's Manual teaches a low voltage differential signal ("LVDS") channel. Pet. 51; Ex. 1019, 3. According to Petitioner, the LVDS Owner's Manual teaches that an LVDS channel can be used for peripheral links and rack-to-rack systems, and, thus, it would have been obvious to use the LVDS channel taught by the LVDS Owner's Manual for the peripheral links in the rack-to-rack system in Horst. Pet. 51–52; Ex. 1019, 8.

Patent Owner argues that Petitioner fails to explain how the teachings of the LVDS Owner's Manual would have been combined with Horst. Prelim. Resp. 47–48. Patent Owner's argument is not persuasive. As discussed above, Petitioner explains that Horst uses a differential signal channel, and that the LVDS Owner's Manual teaches a specific type of differential signal channel, namely an LVDS channel, that is suitable for systems like the one in Horst. Thus, on this record, Petitioner demonstrates that one of ordinary skill in the art would have had sufficient reason to use the LVDS channel taught by the LVDS Owner's Manual as the differential signal channel in the system taught by Horst.

Independent claim 24 recites that the LVDS channel transmits "encoded data of Peripheral Component Interconnect (PCI) bus transaction." Ex. 1001, col. 27, ll. 21–26. Petitioner argues that the TNet bus interface in Horst encodes the information transmitted on the byte-serial data links. Pet. 32–33; Ex. 1009, Fig. 4 ("8B/9B encoder"). Petitioner also argues that the TNet bus interface communicates with peripheral devices that use PCI industry standard buses. Pet. 31–32; Ex. 1009, 7 ("Different versions of the

bus interface logic support industry standard buses such as VME and the peripheral component interconnect (PCI).”). Patent Owner argues that Petitioner’s overly broad construction of the term “Peripheral Component Interconnect (PCI) bus transaction” is fatal to Petitioner’s reliance on Horst. Prelim. Resp. 10–11. Patent Owner does not address, however, the portion of Horst discussed above that expressly discloses communicating with peripheral devices that use PCI industry standard buses. On this record, Petitioner has shown sufficiently that the combination of Horst and the LVDS Owner’s Manual teaches the above limitation of claim 24.

Independent claim 24 recites that the ACM comprises “a microprocessor unit coupled to a mass memory storage device.” Ex. 1001, col. 27, ll. 26–28. Petitioner argues that the processor node in Horst includes a CPU coupled to SCSI disks. Pet. 31; Ex. 1009, Fig. 2. On this record, Petitioner has shown sufficiently that Horst teaches the above limitation of claim 24.

Independent claim 24 recites that the ACM comprises “a north bridge to communicate address and data bits of PCI bus transaction in serial form, said north bridge directly coupled to said microprocessor unit.” Ex. 1001, col. 27, ll. 29–31. Petitioner argues that the TNet processor interface in Horst is a north bridge that is directly coupled to the CPU. Pet. 31–32; Ex. 1009, Fig. 7. Petitioner argues that the TNet processor interface in Horst includes a set of byte-seral data links similar to those discussed above with respect to the TNet bus interface. Pet. 31–32; Ex. 1009, 3, Figs. 3, 4, 7. Also, as discussed above, Petitioner argues that the TNet processor interface communicates with peripheral devices that use PCI industry standard buses. Pet. 31–32; Ex. 1009, 7 (“Different versions of the bus interface logic

support industry standard buses such as VME and the peripheral component interconnect (PCI).”). On this record, Petitioner has shown sufficiently that Horst teaches the above limitation of claim 24.

Independent claim 24 recites that the ACM comprises “a main memory coupled to said microprocessor unit through said north bridge.” Ex. 1001, col. 27, ll. 32–33. Petitioner argues that the processor node in Horst includes a main memory coupled to the CPU through the TNet processor interface. Pet. 32; Ex. 1011, Fig. 7. On this record, Petitioner has shown sufficiently that Horst teaches the above limitation of claim 24.

Independent claim 24 recites that the ACM comprises “a second LVDS channel comprising two unidirectional serial channels that transmit data in opposite directions, said second LVDS channel extending from said north bridge to convey said address and data bits of PCI bus transaction in serial form.” Ex. 1001, col. 27, ll. 34–38. Petitioner argues that the TNet processor interface in Horst includes a set of byte-serial data links similar to those discussed above with respect to the TNet bus interface. Pet. 33; Ex. 1009, 3, Figs. 3, 4, 7. On this record, Petitioner has shown sufficiently that Horst teaches the above limitation of claim 24.

Independent claim 24 recites “applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device.” Ex. 1001, col. 27, ll. 39–41. Petitioner argues that Mathers teaches a security program for a hard disk drive that is activated upon power-up of the hard disk drive. Pet. 24, 34; Ex. 1014, col. 1, ll. 44–46, col. 6, ll. 24–27. Petitioner argues that it would have been obvious to combine the security program in Mathers with the TNet system in Horst in order to control unauthorized access to the mass memory

storage device in Horst. Pet. 34. On this record, Petitioner has shown sufficiently that the combination of Horst and Mathers teaches the above limitation of claim 24.

Independent claim 24 recites "prompting for a user password from a user on a LCD display coupled to the console." Ex. 1001, col. 27, ll. 42–43. Petitioner argues that Mathers teaches a security program that prompts a user for a password. Pet. 25, 34; Ex. 1014, col. 4, ll. 6–9, Fig. 4. Petitioner argues that a person of ordinary skill in the art would have known that a LCD display could be used to prompt the user for a password. Pet. 25; Ex. 1003 ¶¶ 134, 140[24F]. On this record, Petitioner has shown sufficiently that the combination of Horst and Mathers teaches the above limitation of claim 24. Therefore, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 24 would have been obvious over Horst, Mathers, and the LVDS Owner's Manual.

b. *Claims 31–33*

Independent claim 31 recites limitations similar to those addressed above with respect to independent claim 24. Ex. 1001, col. 28, ll. 20–43. Independent claim 31 further recites that the console comprises "a LAN communication device." *Id.* at col. 28, l. 24. Petitioner argues that the cabinet in Horst includes a LAN controller for accessing the Ethernet. Pet. 35; Ex. 1009, Fig. 2. On this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 31 would have been obvious over Horst, Mathers, and the LVDS Owner's Manual.

Dependent claim 32 depends from claim 31 and further recites that "said mass memory storage device comprises a flash memory." Ex. 1001, col. 28, ll. 44–45. Petitioner argues that the password for the security

program in Mathers can be stored in a flash memory on the hard disk drive electronics board. Pet. 27, 35; Ex. 1014, col. 1, ll. 58–61. As discussed above, Petitioner argues that it would have been obvious to combine the security program in Mathers with the system in Horst in order to control unauthorized access to the mass memory storage device in Horst. Pet. 34–35. Petitioner also argues that it specifically would have been obvious to combine the flash memory in Mathers with Horst because flash memory is faster and uses less power than a traditional hard disk drive. Pet. 35.

Patent Owner argues that Petitioner does not explain how or why one of ordinary skill in the art would have combined the flash memory in Mathers with the SCSI disks in Horst. Prelim. Resp. 39–42. Specifically, Patent Owner argues that Petitioner does not demonstrate why one of ordinary skill in the art would replace the large, writable disks in Horst with the small, non-writable flash memory in Mathers. Prelim. Resp. 40–41. Patent Owner's argument is not persuasive. Mathers teaches storing the password for the security program in a flash memory that is on the same electronics board as the hard disk drive. Thus, the combination proposed by Petitioner involved adding a flash memory to the SCSI disks in Horst, not replacing the SCSI disks with a flash memory. On this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 32 would have been obvious over Horst, Mathers, and the LVDS Owner's Manual.

Dependent claim 33 depends from claim 31 and further recites "entering the user password from a keyboard coupled to the console." Ex. 1001, col. 28, ll. 46–47. Petitioner argues that, in Mathers, the password is entered from the keyboard of a computer in which the hard disk drive is

installed. Pet. 36; Ex. 1014, col. 4, ll. 6–9. On this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 33 would have been obvious over Horst, Mathers, and the LVDS Owner's Manual.

4. *Obviousness of Claims 24 and 31–33 over Bogaerts, Gulick, Mathers, and James*

Petitioner argues that claims 24 and 31–33 would have been obvious over Bogaerts, Gulick, Mathers, and James. Pet. 59. Bogaerts relates to a scalable coherent interface for data acquisition. Ex. 1011, 1. We have reviewed Petitioner's assertions and supporting evidence, and, for the reasons discussed below, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claims 31–33 would have been obvious over Bogaerts, Gulick, Mathers, and James. Petitioner does *not* demonstrate, however, a reasonable likelihood of prevailing in showing that claim 24 would have been obvious over Bogaerts, Gulick, Mathers, and James.

a. *Bogaerts as Prior Art*

Petitioner argues that Bogaerts was published on October 2, 1996, and, therefore, constitutes a prior art printed publication under 35 U.S.C. § 102(b). Pet. 58. The evidence of record indicates that Bogaerts was publicly accessible as of October 1996. Specifically, the first page of Bogaerts contains the date "2 October 1996." Ex. 1011, 1. Bogaerts also includes a bar code from the CERN Libraries in Geneva, indicating that it could have been accessed from that library. *Id.* Further, Bogaerts includes the index number "CERN/LHCC LHCC 96-33," indicating that it was indexed by the CERN Libraries in 1996. *Id.*

Patent Owner argues that the October 2, 1996 date on the first page of Bogaerts alone does not establish public accessibility. Prelim. Resp. 18.

Patent Owner's argument is not persuasive, because, as discussed above, Bogaerts contains other indicia of public accessibility. Patent Owner also argues that Bogaerts is a preliminary status report, and, thus, it was "not publication-ready." Prelim. Resp. 19–20. Patent Owner's argument is not persuasive. Bogaerts is labeled a preliminary status report because it contains "incomplete milestone measurements due to delay in delivery of SCI equipment." Ex. 1011, 1 n.1. As such, Bogaerts indicates that the measurements discussed therein may be preliminary, but does not indicate that the report itself is unfinished. As discussed above, the evidence of record indicates that Bogaerts was publicly accessible as of October 1996.[3] Therefore, on this record, Petitioner has shown sufficiently that Bogaerts is a prior art printed publication under § 102(b).

b. *Claim 24*

Independent claim 24 recites "encoded data of Peripheral Component Interconnect (PCI) bus transaction." Ex. 1001, col. 27, ll. 24–25. Petitioner does not identify with specificity anything in Bogaerts that teaches or suggests that the data of a PCI bus transaction is *encoded*. Pet. 46. Further, the parts of Mr. Young's Declaration cited by Petitioner do not persuade us that Bogaerts teaches or suggests that the data of PCI bus transaction is encoded. Ex. 1003 ¶¶ 162, 168–170, 200[24B]. One paragraph of Mr. Young's Declaration states that a person of ordinary skill in the art at the time "would also understand that, for the system to be able to interface with those peripheral components over a serial bus, the addressing and data

[3] Pursuant to our Order dated January 13, 2015, we do not consider Ex. 2004 or Patent Owner's arguments relating thereto for purposes of this decision. Paper 9, 2–3.

would need to be encoded." *Id.* ¶ 170. However, Mr. Young does not provide a sufficient explanation or credible evidence to support that conclusory statement. *Id.* Therefore, on this record, Petitioner does *not* demonstrate a reasonable likelihood of prevailing in showing that claim 24 would have been obvious over Bogaerts, Gulick, Mathers, and James.[4]

c. *Claims 31–33*

Independent claim 31 recites "inserting an attached computer module ("ACM") into a bay of a console in a modular computer system." Ex. 1001, col. 28, ll. 22–23. Petitioner identifies the SMP node in Figure 13 of Bogaerts as being the ACM, and the SCI switch, disk subsystem, and I/O expansion in Figure 13 as being the console. Pet. 37–39; Ex. 1011, Fig. 13. Petitioner also identifies the VME module in Figure 15 of Bogaerts as being the ACM, and a VME crate as being the console. Pet. 37–39; Ex. 1011, Fig. 15. Petitioner argues that it would have been obvious to one of ordinary skill in the art to insert the ACM into the console through rack mounting. Pet. 38–39; Ex. 1003 ¶¶ 165, 200[31A]. On this record, Petitioner has shown sufficiently that Bogaerts teaches the above limitation of claim 31.

Independent claim 31 recites "said console comprising a LAN communication device and a first low voltage differential signal (LVDS) channel comprising two sets of unidirectional serial channels that transmit data in opposite directions." Ex. 1001, col. 28, ll. 23–27. Petitioner argues that it would have been obvious to one of ordinary skill in the art that the I/O expansion in the console of Bogaerts could include a LAN communication device. Pet. 49; Ex. 1003 ¶¶ 174, 175, 200[31A(i)]. Petitioner argues that

[4] Petitioner does not argue that it would have been obvious to combine an encoding feature from Gulick, Mathers, or James with Bogaerts. Pet. 46.

the components in the console in Bogaerts communicate via LC-2 controllers that use an LVDS channel. Pet. 46; Ex. 1011, 7 ("LC-2 . . . uses for a first time LVDS signals."). Further, Petitioner argues that LC-2 controllers communicate using two sets of unidirectional serial channels that transmit in opposite directions. Pet. 46; Ex. 1011, Fig. 14; Ex. 1003 ¶ 200[31(A)(ii)]. On this record, Petitioner has shown sufficiently that Bogaerts teaches the above limitation of claim 31.

Independent claim 31 recites that the ACM comprises "a microprocessor unit coupled to a mass memory storage device." Ex. 1001, col. 28, ll. 27–30. Petitioner argues that the SMP node in Bogaerts includes a CPU coupled to a disk subsystem. Pet. 39; Ex. 1011, Fig. 13. On this record, Petitioner has shown sufficiently that Bogaerts teaches the above limitation of claim 31.

Independent claim 31 recites that the ACM comprises "a second LVDS channel comprising two sets of unidirectional serial channels that transmit data in opposite directions." Ex. 1001, col. 28, ll. 31–33. Petitioner argues that the SMP node in Bogaerts includes LC-2 controllers similar to those discussed above with respect to the console. Pet. 47; Ex. 1011, Figs. 13, 14. On this record, Petitioner has shown sufficiently that Bogaerts teaches the above limitation of claim 31.

Independent claim 31 recites that the ACM comprises "a peripheral bridge coupled to said microprocessor unit without any intervening Peripheral Component Interconnect (PCI) bus, said peripheral bridge coupled to said second LVDS channel to communicate address and data bits of PCI bus transaction in serial form over said second LVDS channel." Ex. 1001, col. 28, ll. 34–39. Petitioner argues that the PRO-SCI board in

Bogaerts is a peripheral bridge that is coupled to the CPU in Figure 13 without any intervening PCI bus. Pet. 40–41; Ex. 1011, Figs. 13, 14. Petitioner also argues that the PRO-SCI board is coupled to an LVDS channel using the LC-2 controllers (Pet. 47; Ex. 1011, 7 ("LC-2 . . . uses for a first time LVDS signals.")), and communicates through the LVDS channel with devices that use PCI industry standard buses (Pet. 47; Ex. 1011, Fig. 13). Patent Owner argues that Petitioner does not explain how or why one of ordinary skill in the art would have combined James or Gulick with Bogaerts to obtain a peripheral bridge coupled to a microprocessor without any intervening PCI bus. Prelim. Resp. 42–45. Because Petitioner has shown sufficiently that Bogaerts teaches a peripheral bridge coupled to a microprocessor without any intervening PCI bus, for purposes of this decision, we do not rely on Petitioner's alleged rationale for combining James or Gulick with Bogaerts. On this record, Petitioner has shown sufficiently that Bogaerts teaches the above limitation of claim 31.

Independent claim 31 recites "applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device." Ex. 1001, col. 28, ll. 40–42. Petitioner argues that Mathers teaches a security program for a hard disk drive that is activated upon power-up of the hard disk drive. Pet. 24, 48; Ex. 1014, col. 1, ll. 44–46, col. 6, ll. 24–27. Petitioner argues that it would have been obvious to combine the security program in Mathers with the system in Bogaerts in order to control unauthorized access to the mass memory storage device in Bogaerts. Pet. 48. On this record, Petitioner has shown sufficiently that the combination of Bogaerts and Mathers teaches the above limitation of claim 31.

Independent claim 31 recites "prompting for a user password from a user on a display." Ex. 1001, col. 28, l. 43. Petitioner argues that Mathers teaches a security program that prompts a user for a password. Pet. 25, 48–49; Ex. 1014, col. 4, ll. 6–9, Fig. 4. On this record, Petitioner has shown sufficiently that the combination of Bogaerts and Mathers teaches the above limitation of claim 31. Therefore, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 31 would have been obvious over Bogaerts, Gulick, Mathers, and James.

Dependent claim 32 depends from claim 31 and further recites that "said mass memory storage device comprises a flash memory." Ex. 1001, col. 28, ll. 44–45. Petitioner argues that the password for the security program in Mathers can be stored in a flash memory on the hard disk drive electronics board. Pet. 27, 49–50; Ex. 1014, col. 1, ll. 58–61. As discussed above, Petitioner argues that it would have been obvious to combine the security program in Mathers with the system in Bogaerts in order to control unauthorized access to the mass memory storage device in Bogaerts. Pet. 48. Petitioner also argues that it specifically would have been obvious to combine the flash memory in Mathers with Bogaerts because flash memory is faster and uses less power than a traditional hard disk drive. Pet. 50.

Patent Owner argues that Petitioner does not explain how one of ordinary skill in the art would have combined the flash memory in Mathers with the disk subsystem in Bogaerts. Prelim. Resp. 45–46. Patent Owner's argument is not persuasive. Mathers teaches storing the password for the security program in a flash memory that is on the same electronics board as the hard disk drive. Thus, the combination proposed by Petitioner involved adding a flash memory to the disk subsystem in Bogaerts. On this record,

Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 32 would have been obvious over Bogaerts, Gulick, Mathers, and James.

Dependent claim 33 depends from claim 31 and further recites "entering the user password from a keyboard coupled to the console." Ex. 1001, col. 28, ll. 46–47. Petitioner argues that, in Mathers, the password is entered from the keyboard of a computer in which the hard disk drive is installed. Pet. 50; Ex. 1014, col. 4, ll. 6–9. On this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 33 would have been obvious over Bogaerts, Gulick, Mathers, and James.

5. *Obviousness of Claims 24 and 31–33 over Bogaerts, Gulick, Mathers, James, and LVDS Owner's Manual*

Petitioner argues that claims 24 and 31–33 would have been obvious Bogaerts, Gulick, Mathers, James, and the LVDS Owner's Manual. Pet. 59. With respect to claim 24, Petitioner does not argue that the LVDS Owner's Manual teaches or suggests the limitations discussed above in Section II.B.4.b. Pet. 51–52. Therefore, for the same reasons discussed above in Section II.B.4.b, on this record, Petitioner does *not* demonstrate a reasonable likelihood of prevailing in showing that claim 24 would have been obvious over Bogaerts, Gulick, Mathers, James, and the LVDS Owner's Manual.

With respect to claims 31–33, Petitioner explains that this ground is applicable if the combination of Bogaerts, Gulick, Mathers, and James is found not to teach "a serial LVDS channel that comprises 'two sets of unidirectional serial bit channels which transmit data in opposite directions.'" Pet. 51. As discussed above, Petitioner has shown sufficiently that the combination of Bogaerts, Gulick, Mathers, and James teaches the aforementioned limitation. *See* Section II.B.4.c. Accordingly, we do not

institute an *inter partes* review on this alternative ground proposed by Petitioner. *See* 37 C.F.R. § 42.108(a).

III. CONCLUSION

Petitioner demonstrates a reasonable likelihood of prevailing on its challenge to the patentability of claims 24 and 31–33 of the '814 patent as unpatentable under 35 U.S.C. § 103. At this stage in the proceeding, we have not made a final determination with respect to the patentability of any of the challenged claims.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 24 and 31–33 of the '814 patent on the following grounds:

A. Claims 24 and 31–33 as unpatentable under 35 U.S.C. § 103(a) as obvious over Horst, Mathers, and the LVDS Owner's Manual; and

B. Claims 31–33 as unpatentable under 35 U.S.C. § 103(a) as obvious over Bogaerts, Gulick, Mathers, and James;

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '814 patent is hereby instituted commencing on the entry date of this Order, and, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; and

FURTHER ORDERED that the trial is limited to the grounds identified, and no other grounds are authorized.

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